UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/043,208	01/14/2002	Hiroaki Tamura	401532	6157

23548 7590 02/04/2005

LEYDIG VOIT & MAYER, LTD
700 THIRTEENTH ST. NW
SUITE 300
WASHINGTON, DC 20005-3960

EXAMINER	
DUNCAN, MARC M	

ART UNIT	PAPER NUMBER
2113	

DATE MAILED: 02/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application N .	Applicant(s)	
	10/043,208	TAMURA, HIROAKI	
	Examiner	Art Unit	
	Marc M Duncan	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondenc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 December 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-8 and 10-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *4,5,7,8 and 10-14* is/are allowed.

6)☒ Claim(s) *1 and 3* is/are rejected.

7)☒ Claim(s) *6* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

FINAL REJECTION

Status of the Claims

Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jeddeloh in view of Brauch et al.

Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jeddeloh and Brauch as applied to claim 1 above, and further in view of Kaiser.

Claim 6 is objected to.

Claims 4-5, 7-8 and 10-14 are allowed.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jeddeloh in view of Brauch et al.

Regarding claim 1:

Jeddeloh teaches a first chip having an electrically rewritable nonvolatile memory in col. 2 lines 2-7 and col. 2 line 65-col. 3 line 2.

Jeddeloh teaches a second chip including a memory having therein a redundant circuit in Fig. 1 and col. 2 lines 4-7.

Jeddeloh teaches a substrate on which said first chip and second chip are mounted in Fig. 1 and col. 2 lines 52-62.

Jeddeloh teaches wherein information required for utilizing said redundant circuit in place of a faulty portion in said memory on said second chip is stored in said nonvolatile memory on said first chip, and said redundant circuit is utilized in place of the faulty portion in said memory on said second chip based on the information stored in said nonvolatile memory in col. 2 lines 2-7 and lines 62-65.

Jeddeloh does not explicitly teach wherein said second chip further comprises a circuit for memory test having a nonvolatile memory, wherein said nonvolatile memory of said second chip stores, a test program for detecting whether or not there is a faulty portion in said memory on said second chip; a repair analysis program for identifying the faulty portion when the test program detects that there is a faulty portion in said memory on said second chip, and determining a portion in said redundant circuit that is to be utilized in place of the faulty portion; and a software repair program for writing information required for utilizing the determined portion in said redundant circuit in place of the faulty portion identified by the repair analysis program in said nonvolatile memory on said first chip. Jeddeloh does, however, teach memory chips that have been tested

in order to determine faulty locations so that the faulty locations can be replaced by spare locations.

Brauch teaches wherein said second chip further comprises a circuit for memory test having a nonvolatile memory in Fig. 1 "6."

Brauch teaches a test program for detecting whether or not there is a faulty portion in said memory on said second chip in col. 3 lines 23-26. The BIST functional block necessarily includes a control program, equivalent to the test program of the current claims, stored in a non-volatile memory in order to control execution of the test.

Brauch teaches a repair analysis program for identifying the faulty portion when the test program detects that there is a faulty portion in said memory on said second chip, and determining a portion in said redundant circuit that is to be utilized in place of the faulty portion in col. 3 lines 30-39 and lines 42-48.

Brauch teaches and a software repair program for writing information required for utilizing the determined portion in said redundant circuit in place of the faulty portion identified by the repair analysis program in said nonvolatile memory on said first chip in col. 3 lines 42-48. The device builds a failure bitmap, which is the error map stored in the non-volatile memory of Jeddeloh.

It would have been obvious to one of ordinary skill in the art at the time of invention to combine the test circuit of Brauch with the fault relieving means of Jeddeloh.

One of ordinary skill in the art at the time of invention would have been motivated to combine the teachings because Jeddeloh expresses the need to know which of the

memory locations are faulty. The BIST circuit of Brauch meets this expressed need of Jeddeloh.

Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jeddeloh and Brauch as applied to claim 1 above, and further in view of Kaiser.

Regarding claim 3:

The teachings of Jeddeloh and Brauch are outlined above.

Jeddeloh and Brauch do not explicitly teach the memory of the test circuit being rewritable. Jeddeloh and Brauch do, however, teach running a test program by a controller in order to test the memory device.

Kaiser teaches a rewritable program memory as part of a memory testing circuit in col. 4 lines 10-12.

It would have been obvious to one of ordinary skill in the art at the time of invention to combine the rewritable memory of Kaiser with the memory of Jeddeloh and Brauch.

One of ordinary skill in the art at the time of invention would have been motivated to combine the teachings because Kaiser teaches that a rewritable memory in a memory tester allows multiple different test programs to be run.

Allowable Subject Matter

Claim 6 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

Applicant's arguments filed 12/2/04 have been fully considered but they are not persuasive.

In response to applicant's argument that the examiner is assuming that the Jeddeloh reference does not have any disclosure of separate chips, the examiner disagrees. The first paragraph of the Detailed Description of Jeddeloh clearly state that the memory block 14 is made up of one or more **chips**. This clearly delineates the separation of the memory block 14 and the memory block 16 into more than one chip. It is therefore incorrect for applicant to assert that the examiner is making an inference with no disclosure whatsoever when, in fact, applicant is making an inference that the two blocks are a single chip.

In response to applicant's argument that the examiner is making a mere assertion that Brauch teaches the BIST functional block includes a nonvolatile memory based on an implication, the examiner disagrees. The examiner calls attention to column 3, line 23, which states "BIST functional block 6 is hardware, firmware..." The examiner reminds applicant that firmware, as defined by the Microsoft Computer Dictionary, Third Edition, is "Software routines stored in read-only memory (ROM). Unlike random access memory (RAM), read-only memory stays intact even in the absence of electrical power." Clearly Brauch has an explicit recitation of nonvolatile memory.

Applicant's assertion, therefore, that the examiner's rejection is founded upon one inference piled on a second inference is erroneous and is therefore not persuasive. Furthermore, it is incorrect for applicant to assemble an argument based entirely on

applicant's own opinion of what would support the examiner's purported position and then proceed to attack that argument as a means for attacking the rejection. The rejection must be disproved based on the actual rejection, not on an explanation fabricated by applicant, as is the case in applicant's assumption that the two different kinds of memories on separate chips are separated for ease of manufacturing. If applicant contends that this is true, applicant must show in the references where Jeddeloh or Brauch make such a claim. The rejection is maintained.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Marc M Duncan whose telephone number is 571-272-3646. The examiner can normally be reached on M-T and TH-F 6:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on 571-272-3645. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

md

ROBERT BEAUSOLIEL
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100